Amendments to the Specification:

Replace the paragraph beginning on page 6, line 17 in its entirety with the paragraphs shown below.

Next, a second fetch process 36 requests color information for pixel P1. As bilinear filtering is being employed, this requires the collection of color data from texels ~~T2, T4, T6 and T7~~T0, T1, T2 and T3. As the information relating to the aforementioned pixels is not permanently maintained, the second fetch process 36 sends a request to main memory 22 for the associated pixel information. As the color data associated with pixel P0 has previously been requested by first fetch process 32, the request for information relating to pixel P0 is considered an overlapping request. In a graphics processor containing several interconnected versions of the memory architecture illustrated in FIG. 3, several requests for the same information will quickly overburden and degrade the performance of the main memory 22. In addition, valuable processor time is being wasted as the main memory 22 is required to transmit identical information to at least two different fetch processes. The memory architecture of the present invention overcomes such limitations and the corresponding problems associated therewith by providing more time efficient access to overlapping requests.